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(54) **INTEGRATED CIRCUITS HAVING A PLURALITY OF HIGH-K METAL GATE FETS WITH VARIOUS COMBINATIONS OF CHANNEL FOUNDATION STRUCTURE AND GATE STACK STRUCTURE AND METHODS OF MAKING SAME**

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(58) **Field of Classification Search**
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See application file for complete search history.

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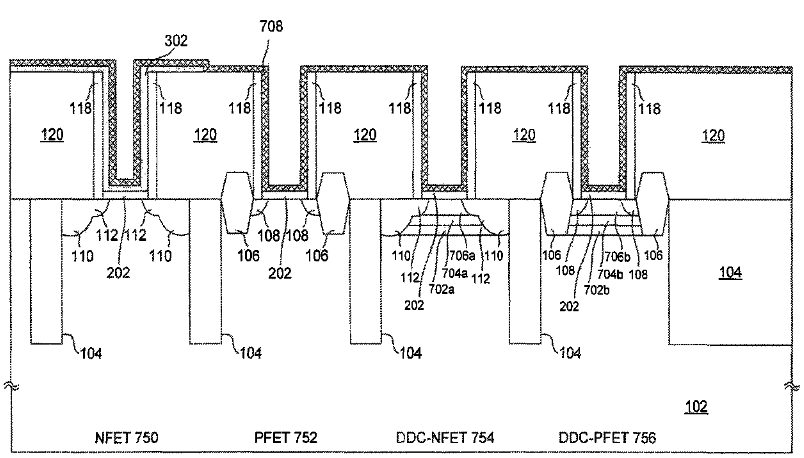
(57) **ABSTRACT**

Semiconductor manufacturing processes include forming conventional channel field effect transistors (FETs) and deeply depleted channel (DDC) FETs on the same substrate and selectively forming a plurality of gate stack types where those different gate stack types are assigned to and formed in connection with one or more of a conventional channel NFET, a conventional channel PFET, a DDC-NFET, and a DDC-PFET in accordance a with a predetermined pattern.

14 Claims, 16 Drawing Sheets



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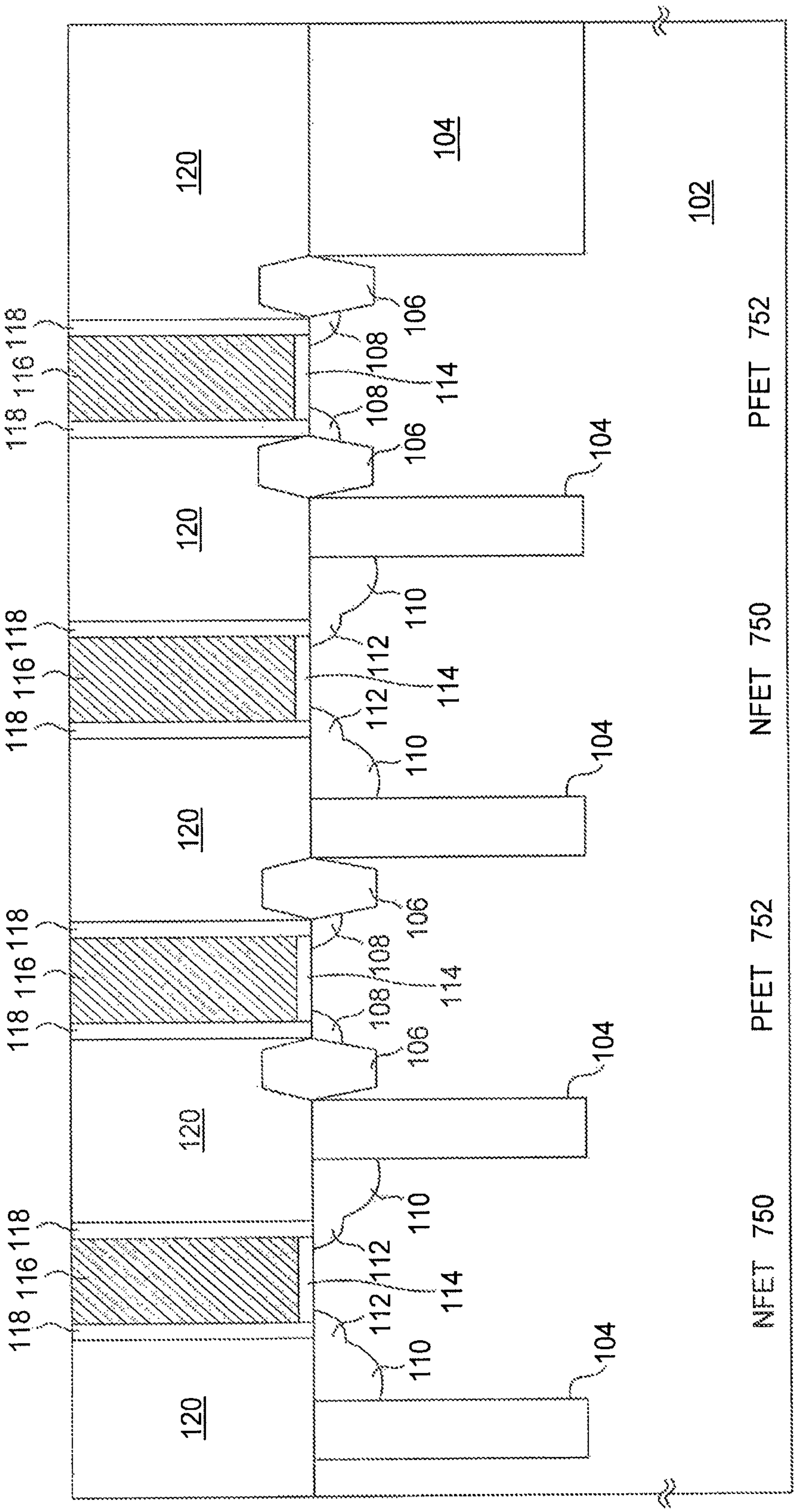


FIG. 1

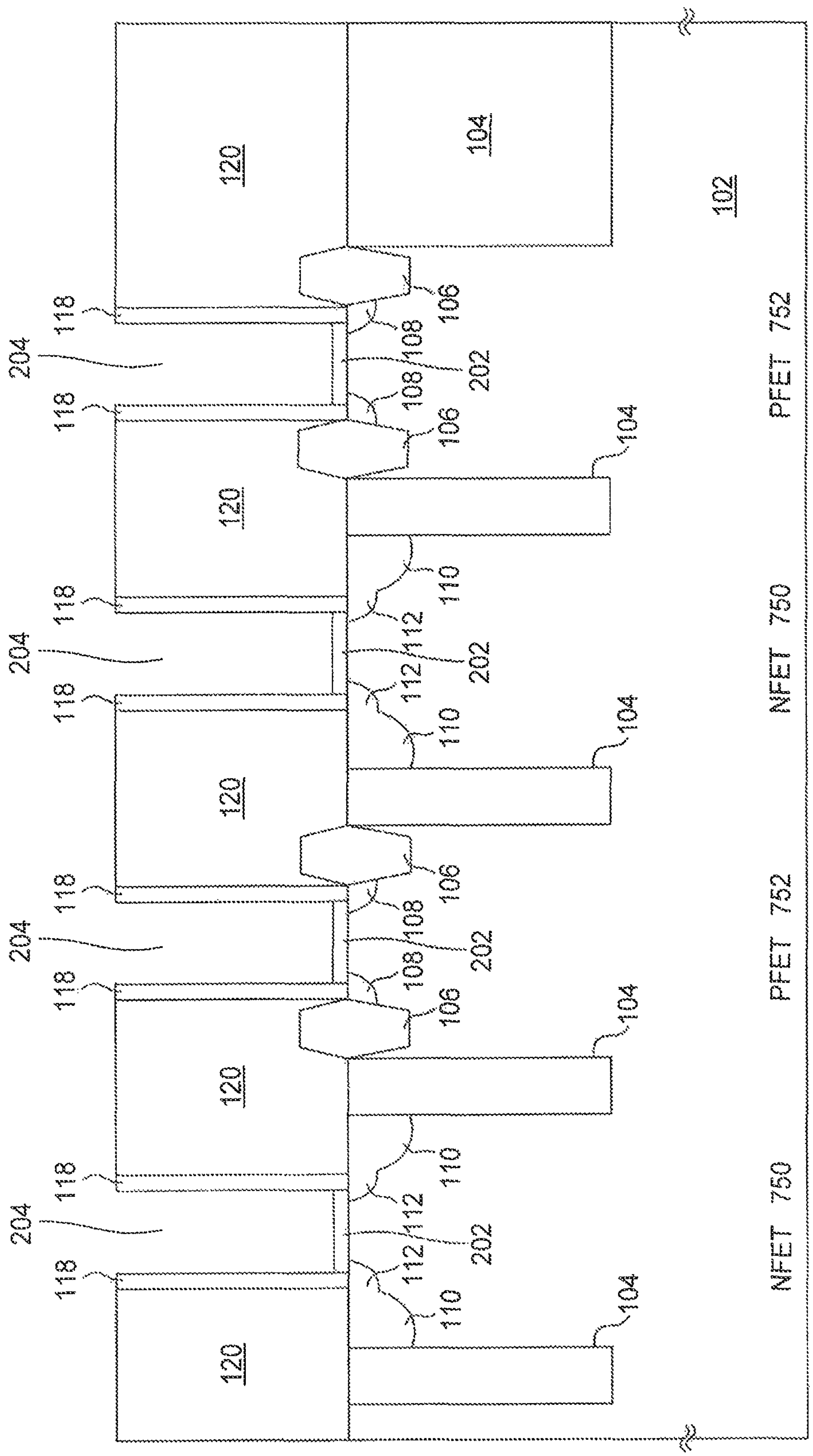


FIG. 2

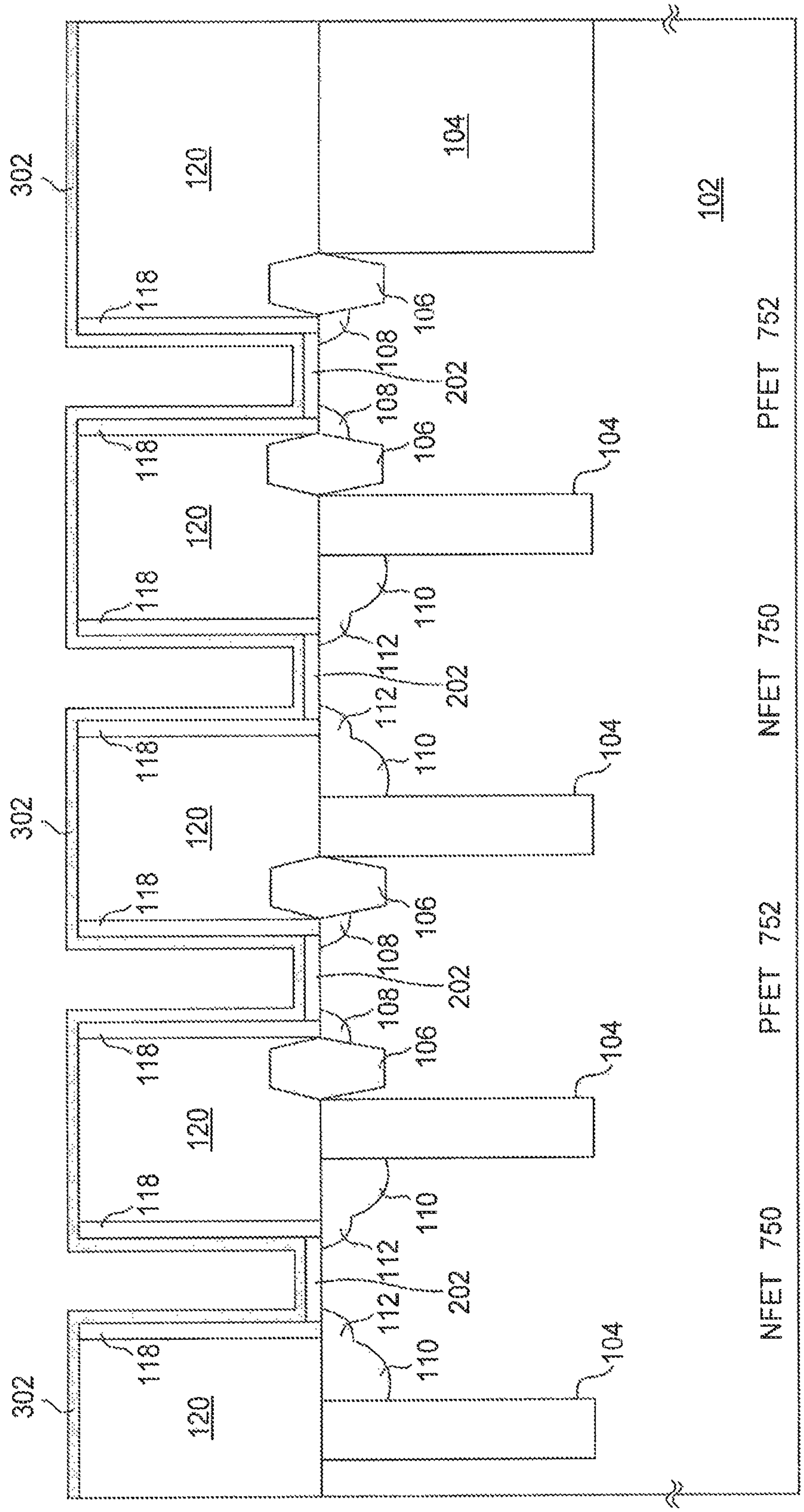


FIG. 3

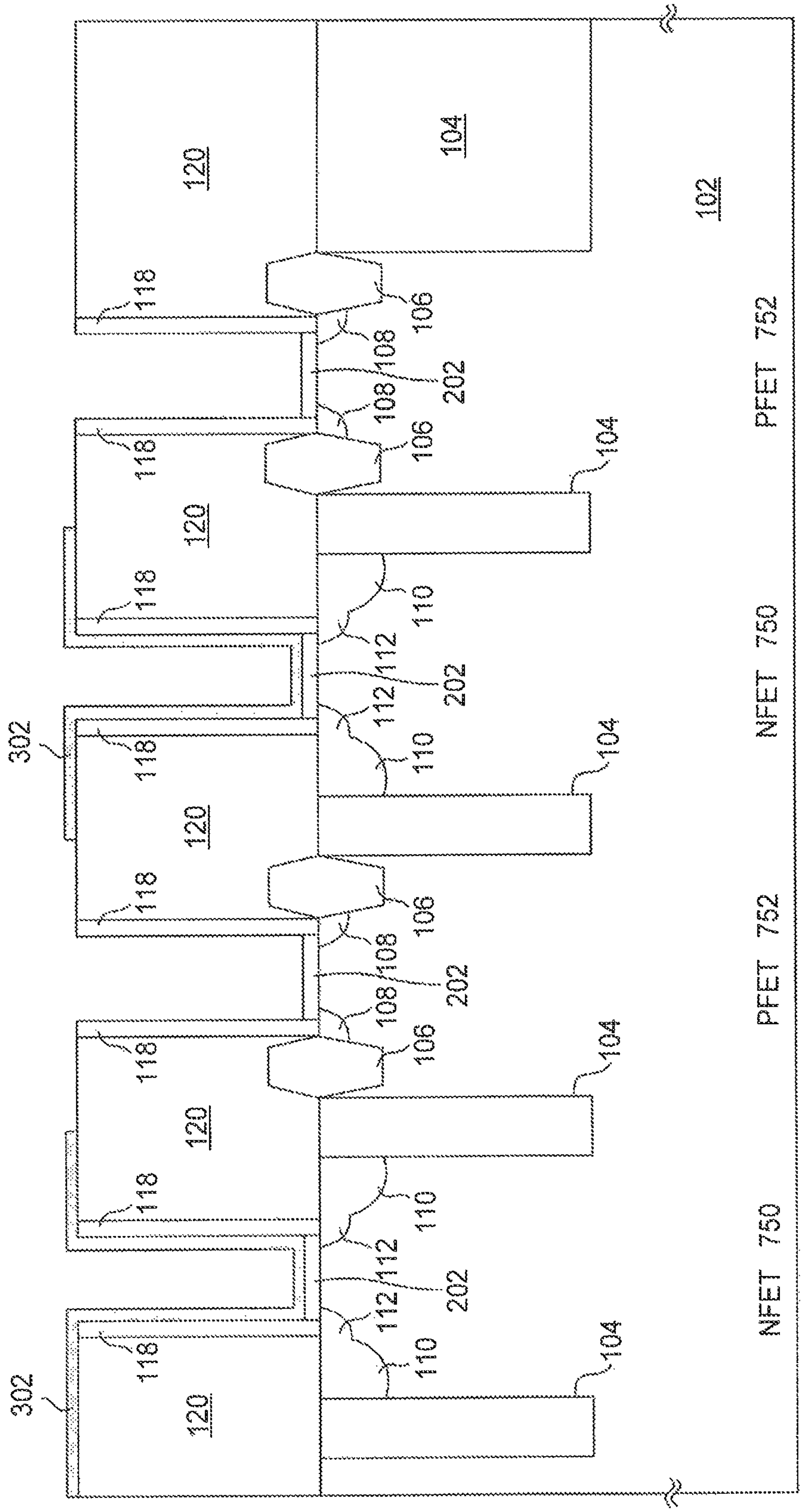


FIG. 4

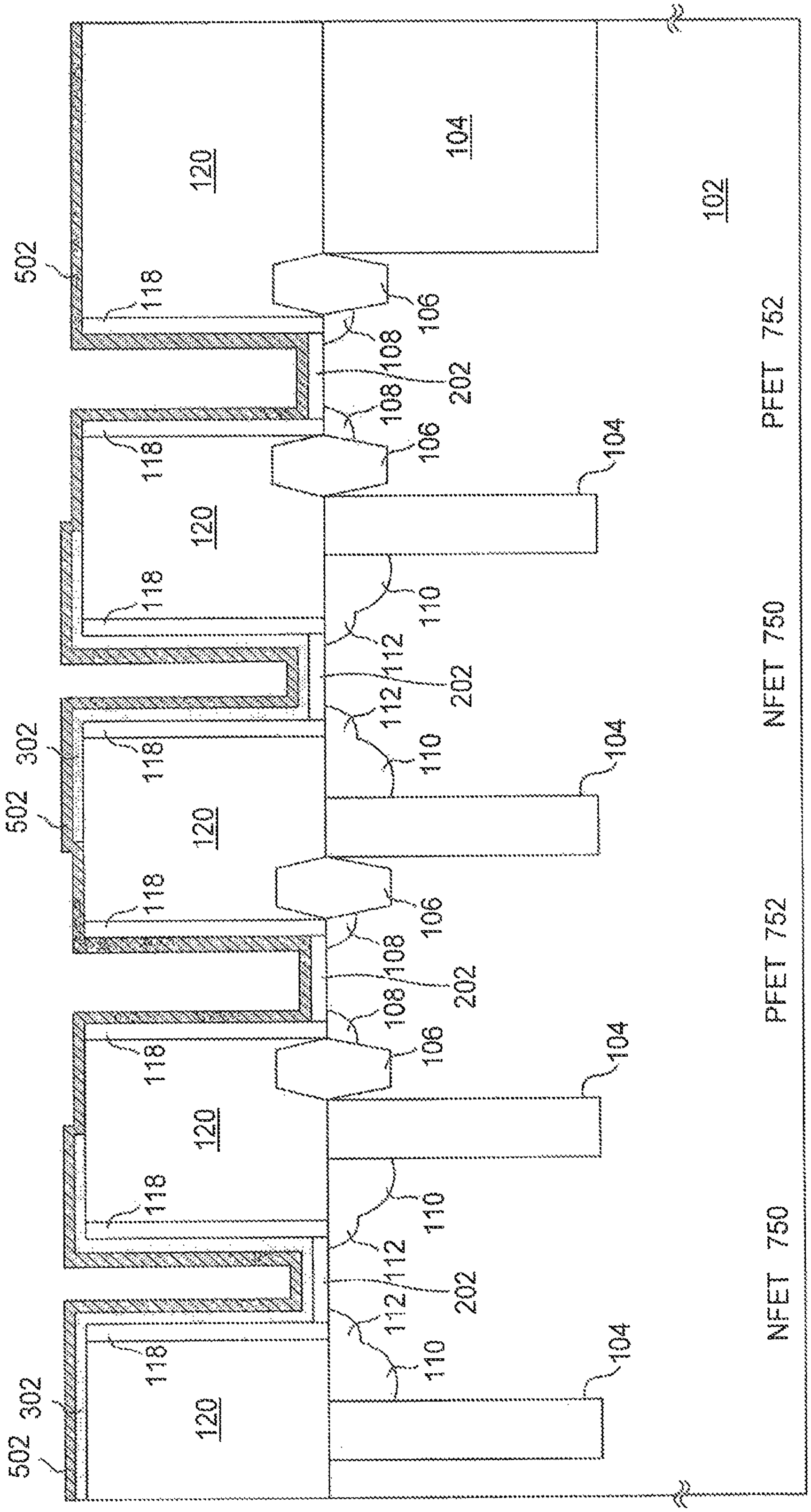


FIG. 5

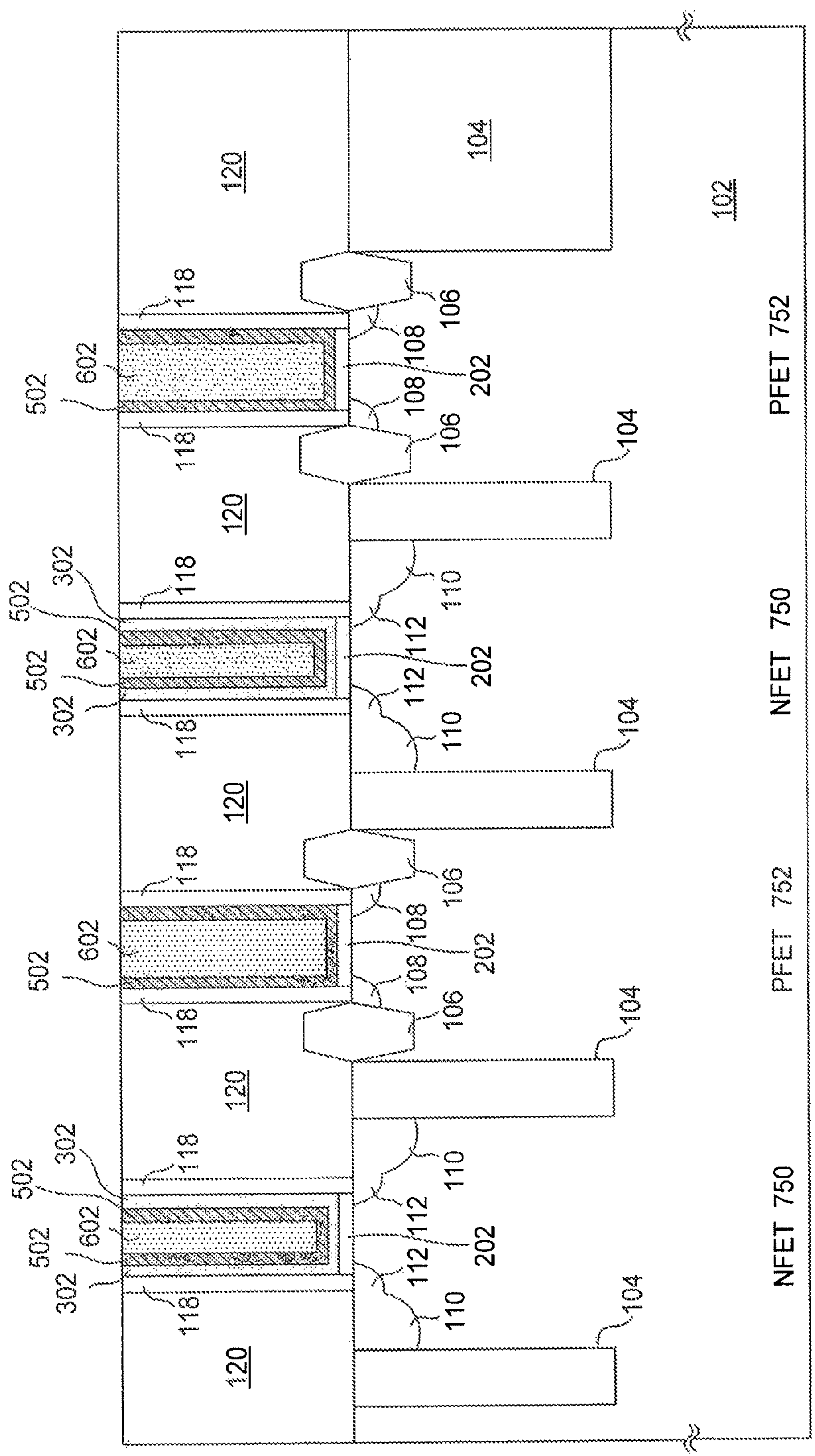

120
104
102
118
106
602
502
108
202
PFET 752
302
110
112
NFET 750

FIG. 6

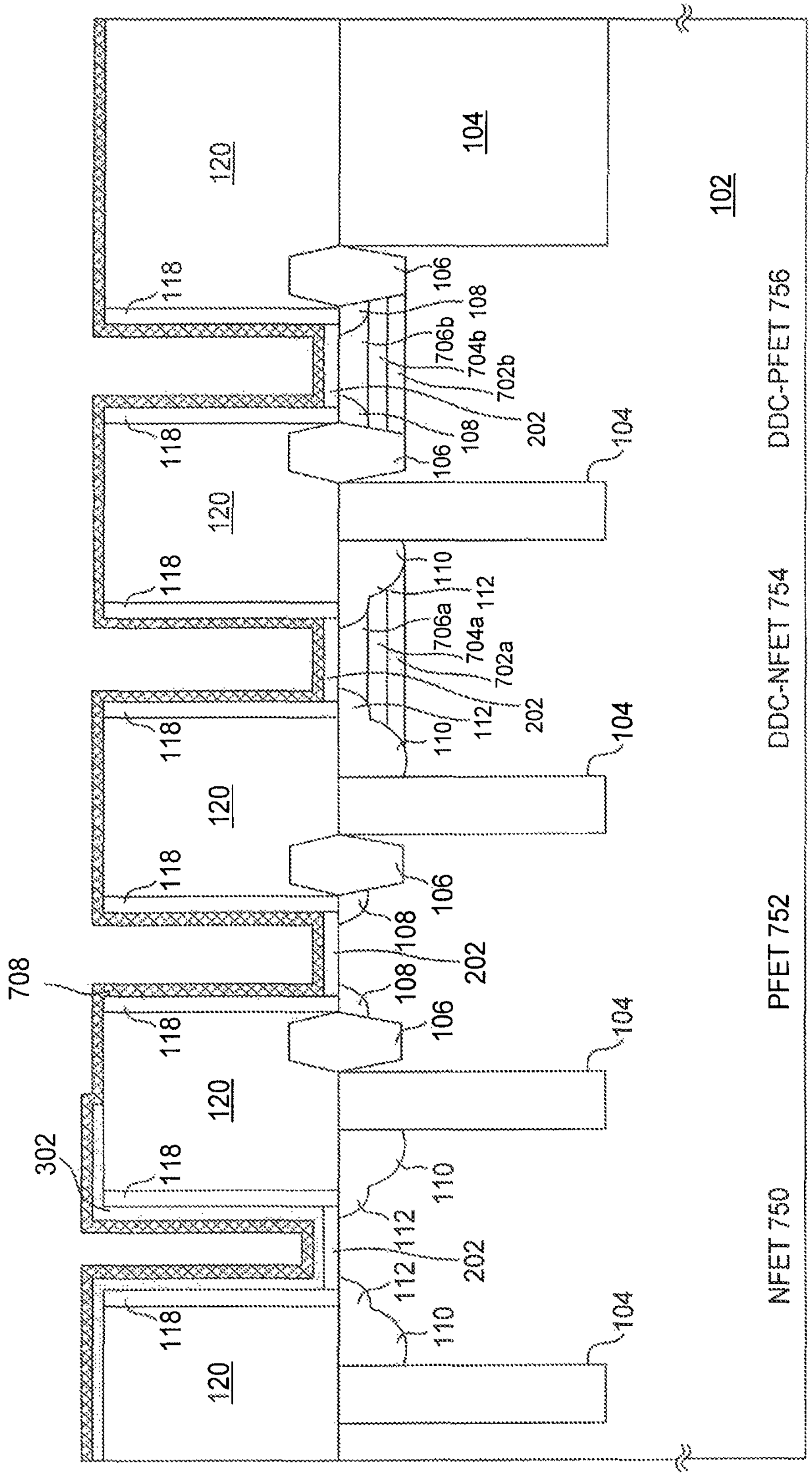
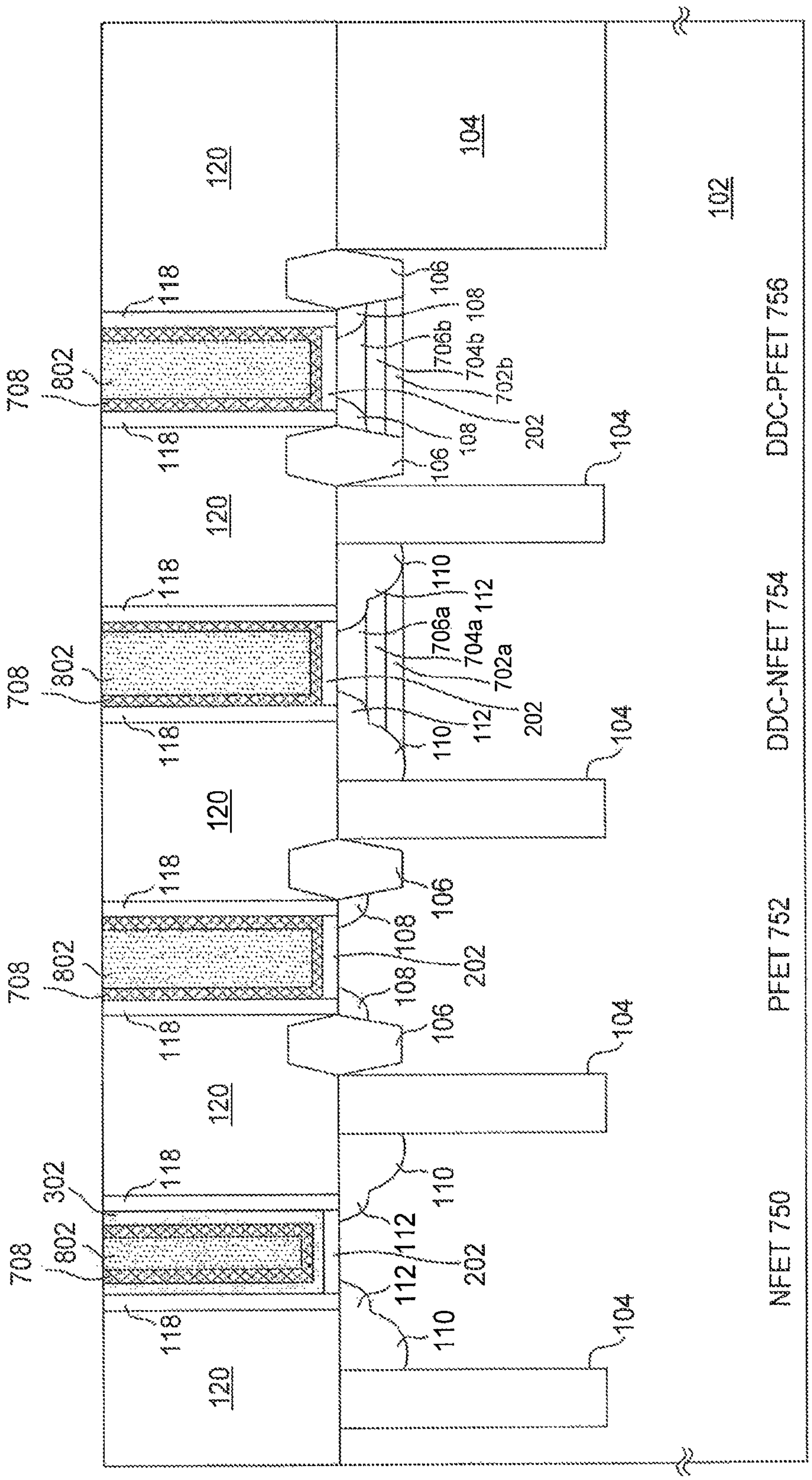
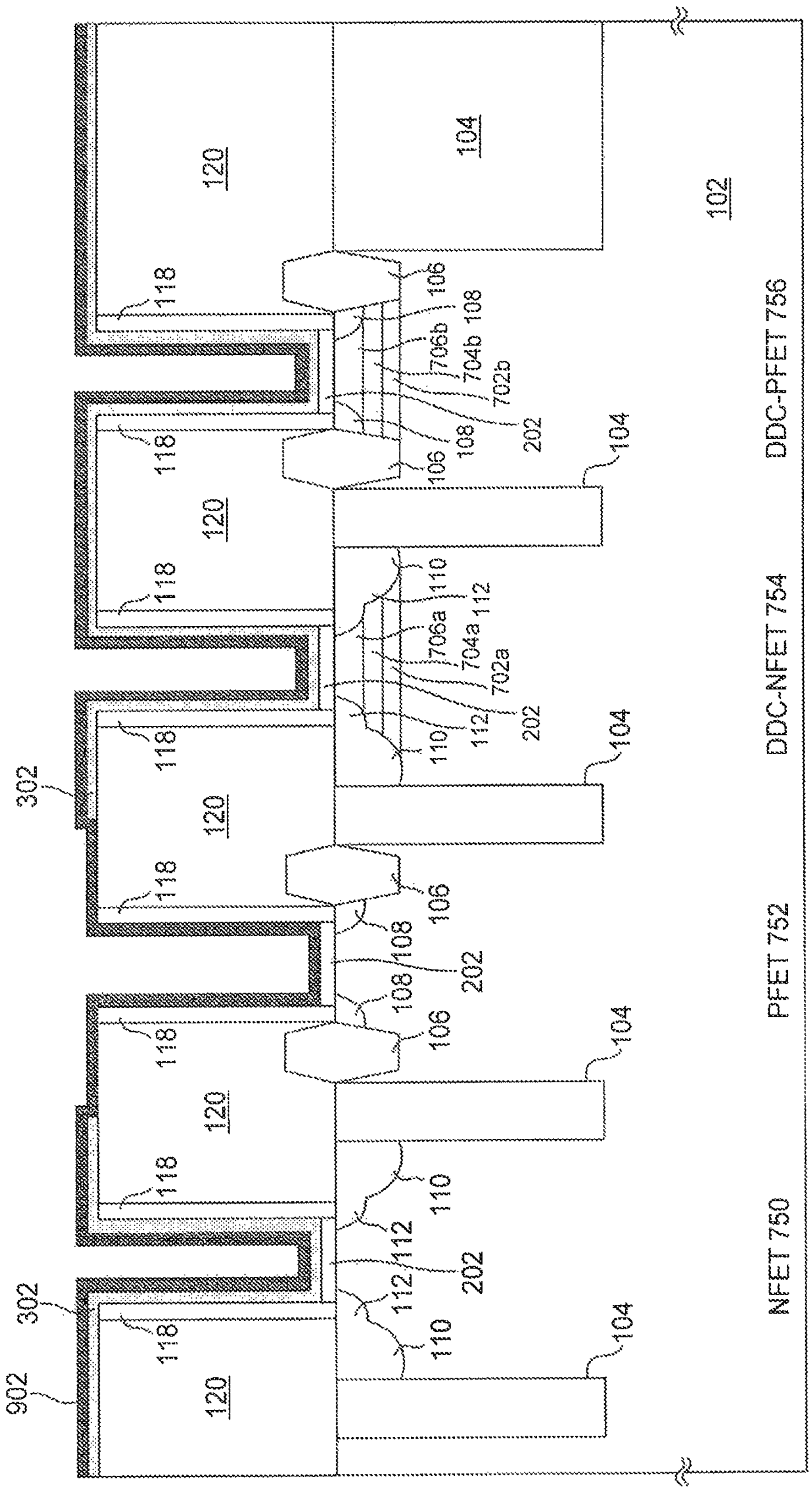

120
104
102
118
106
108
706b
704b
702b
202
DDC-PFET 756
104
110
112
706a
704a
702a
DDC-NFET 754
PFET 752
NFET 750
708
302

FIG. 7



NFET 750
PFET 752
DDC-NFET 754
DDC-PFET 756
102
104
106
108
110
112
118
120
202
302
702a
702b
704a
704b
706a
706b
708
802

FIG. 8



102
104
106
108
110
112
118
120
202
302
902
702a
704a
706a
702b
704b
706b
NFET 750
PFET 752
DDC-NFET 754
DDC-PFET 756

FIG. 9

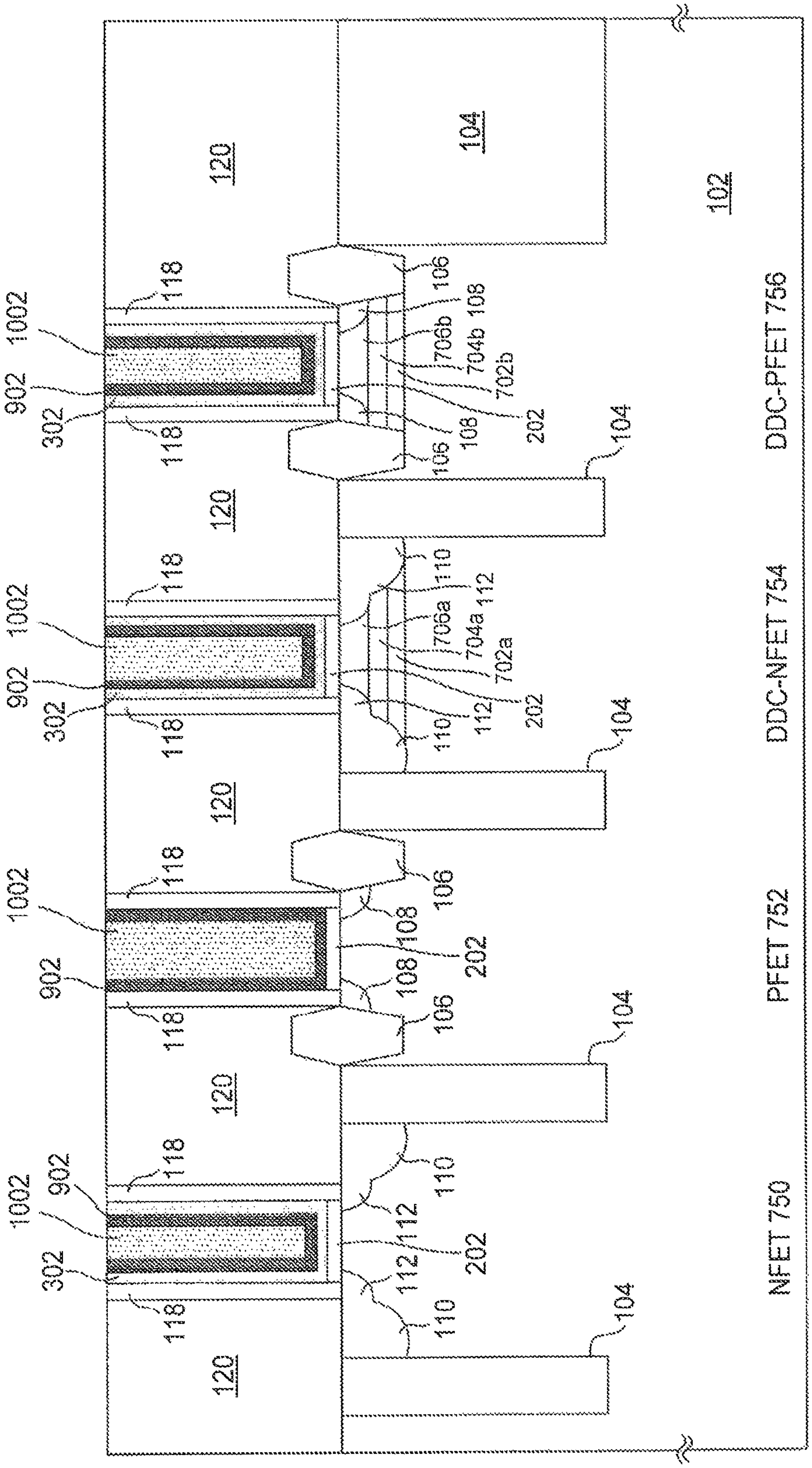
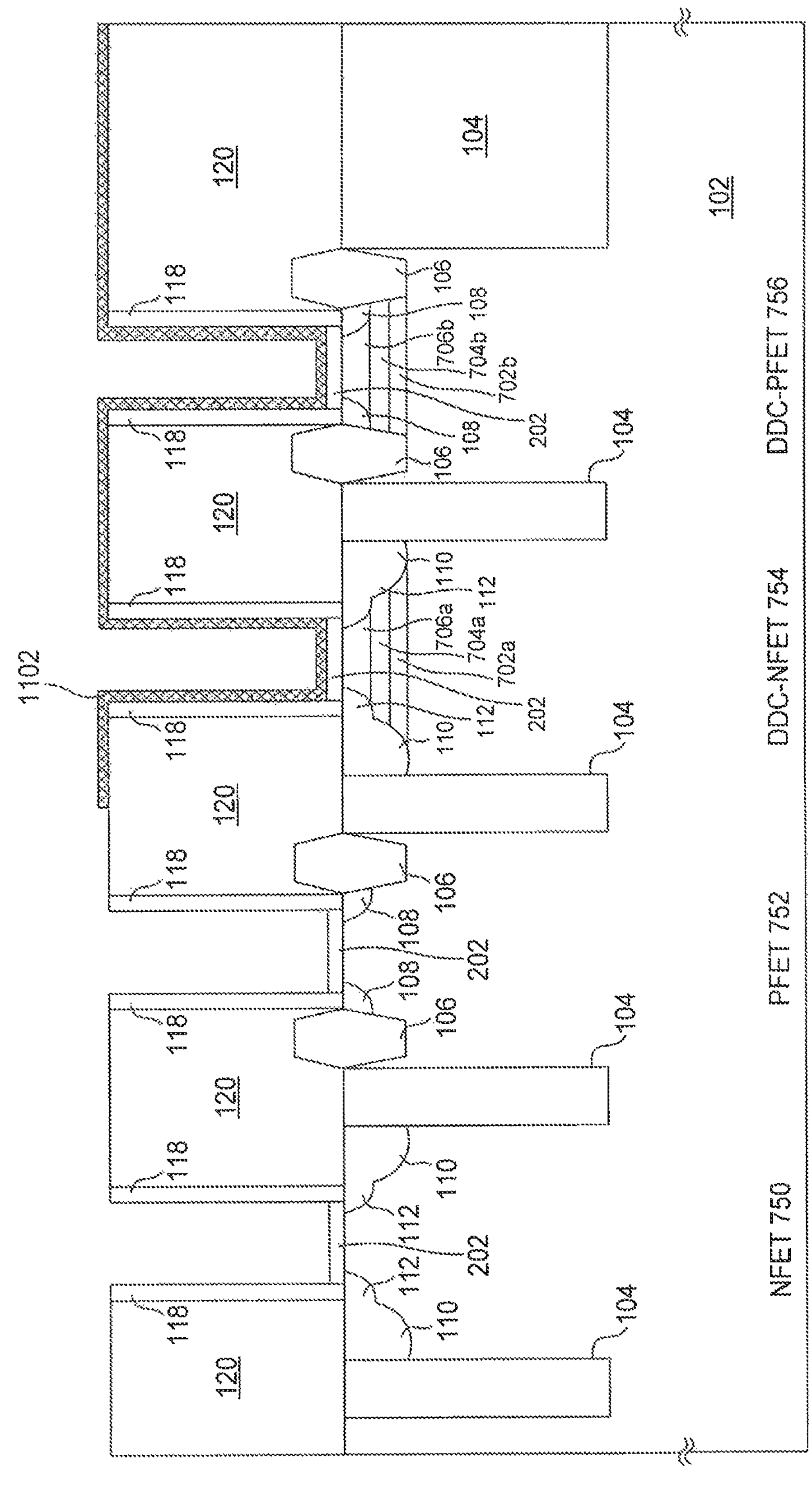
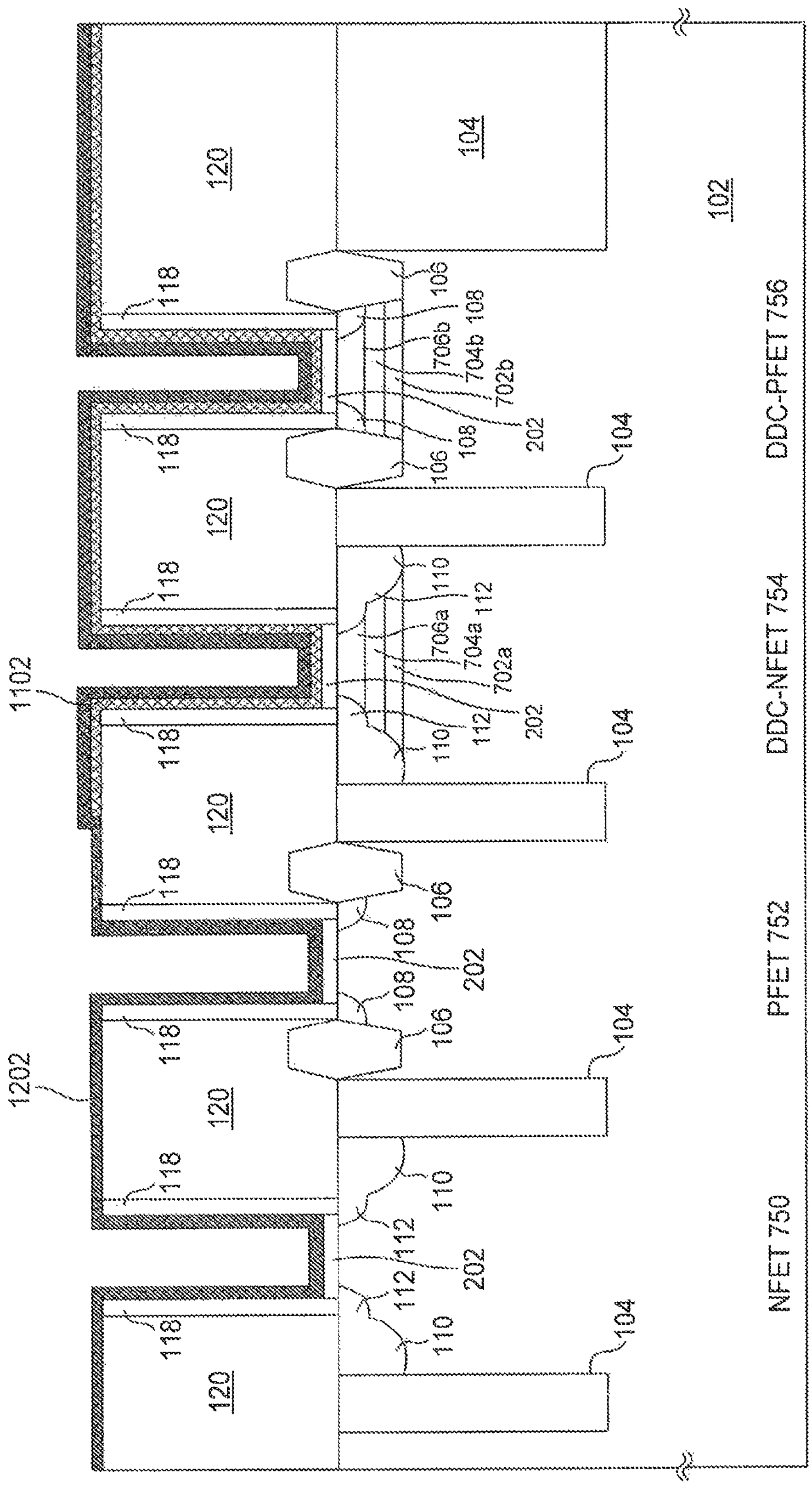

120
104
102
118
1002
902
302
106
108
706b
704b
702b
202
DDC-PFET 756
110
112
706a
704a
702a
DDC-NFET 754
PFET 752
NFET 750

FIG. 10



1102
120
104
102
118
106
108
706b
704b
702b
202
DDC-PFET 756
110
112
706a
704a
702a
DDC-NFET 754
PFET 752
NFET 750

FIG. 11



120
104
102
118
106
108
706b
704b
702b
202
DDC-PFET 756
110
112
706a
704a
702a
DDC-NFET 754
1102
PFET 752
1202
NFET 750

FIG. 12

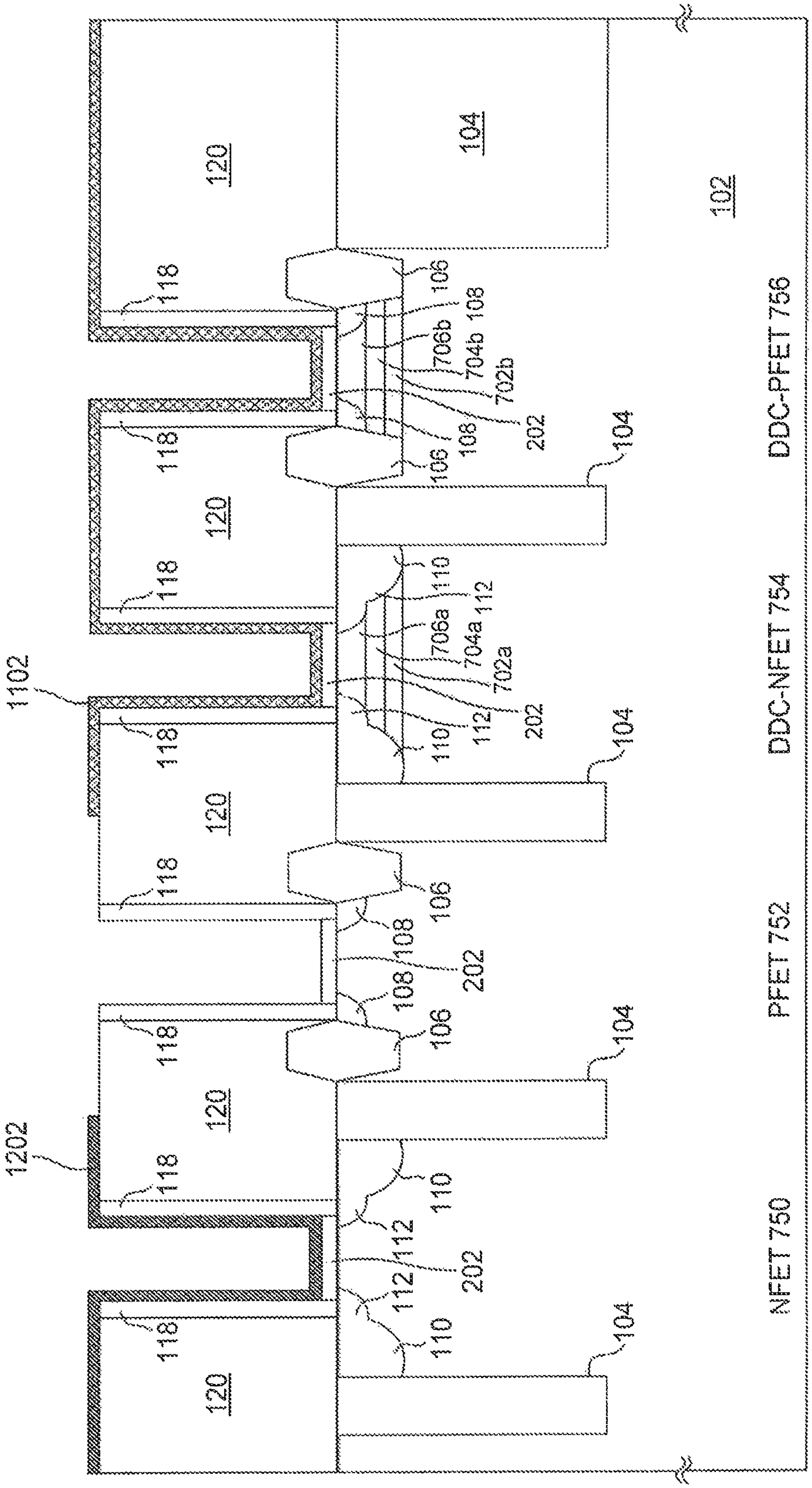

120
104
102
118
106
108
706b
704b
702b
202
104
DDC-PFET 756
120
110
112
706a
704a
702a
DDC-NFET 754
1102
PFET 752
1202
NFET 750

FIG. 13

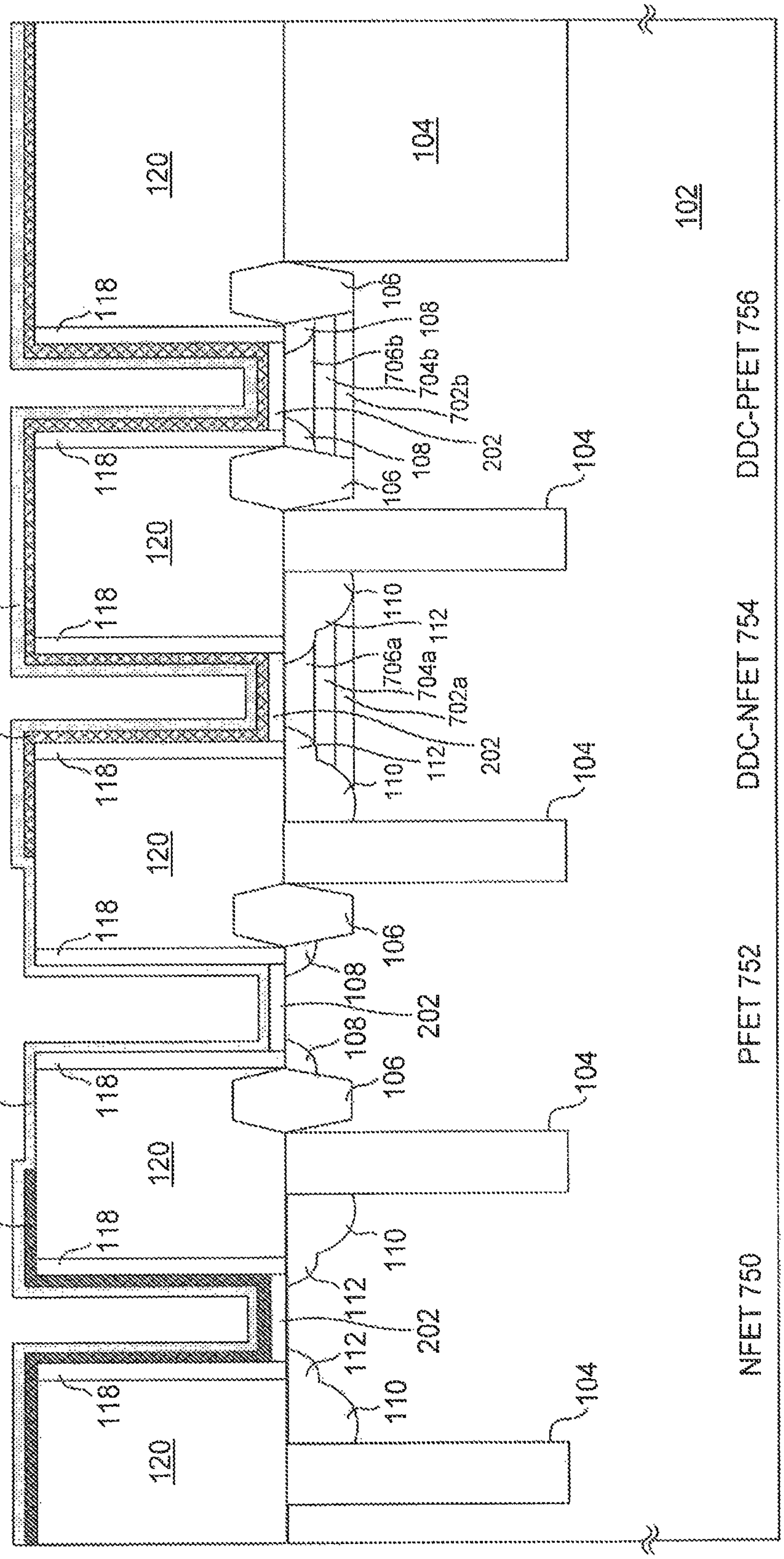

120
104
102
118
106
108
706b
704b
702b
202
DDC-PFET 756
1402
1102
110
112
706a
704a
702a
DDC-NFET 754
PFET 752
1202
NFET 750

FIG. 14

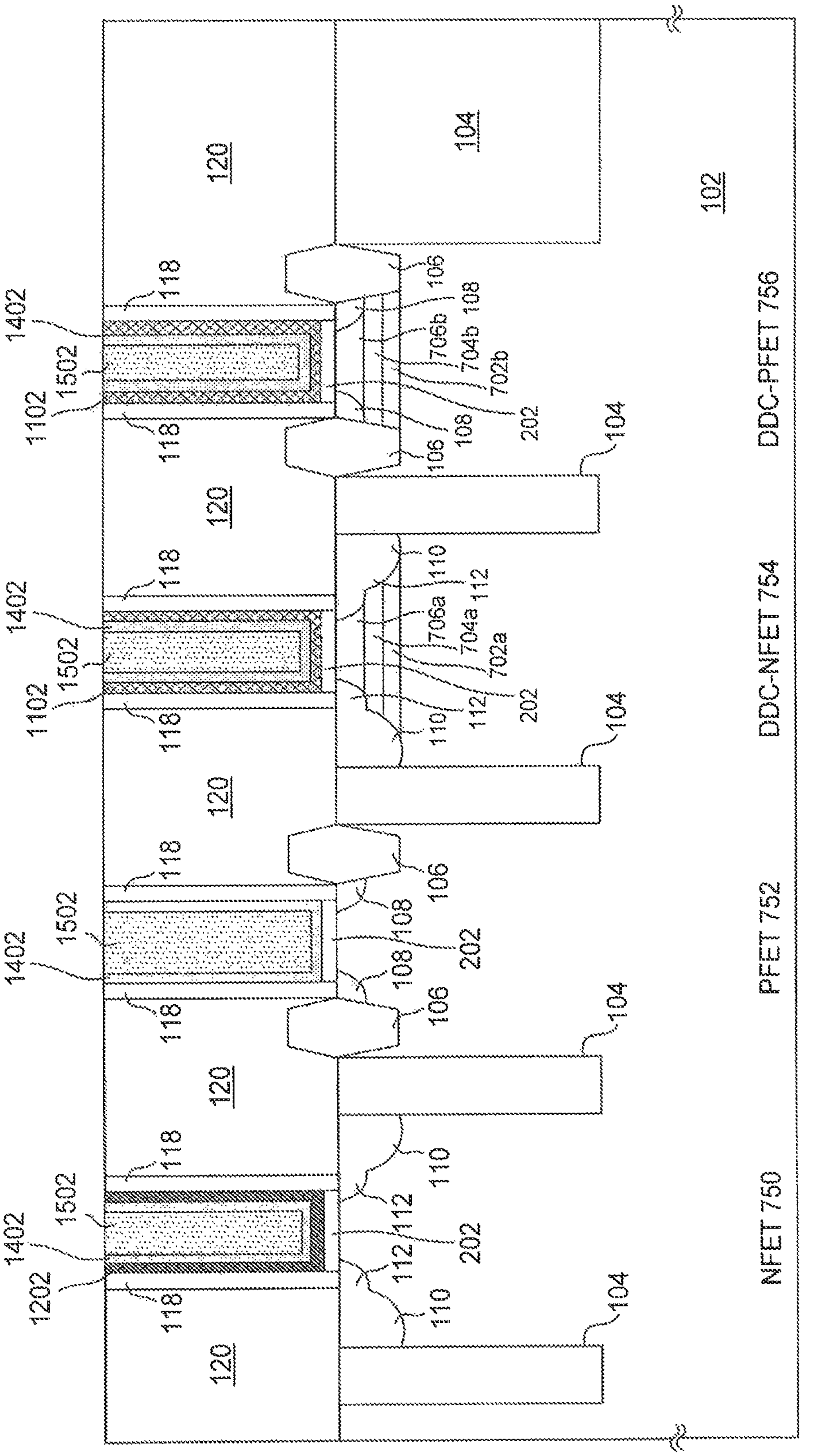

120
104
102
118
1402
1502
1102
106
108
706b
704b
702b
202
DDC-PFET 756
110
112
706a
704a
702a
DDC-NFET 754
PFET 752
1202
NFET 750

FIG. 15

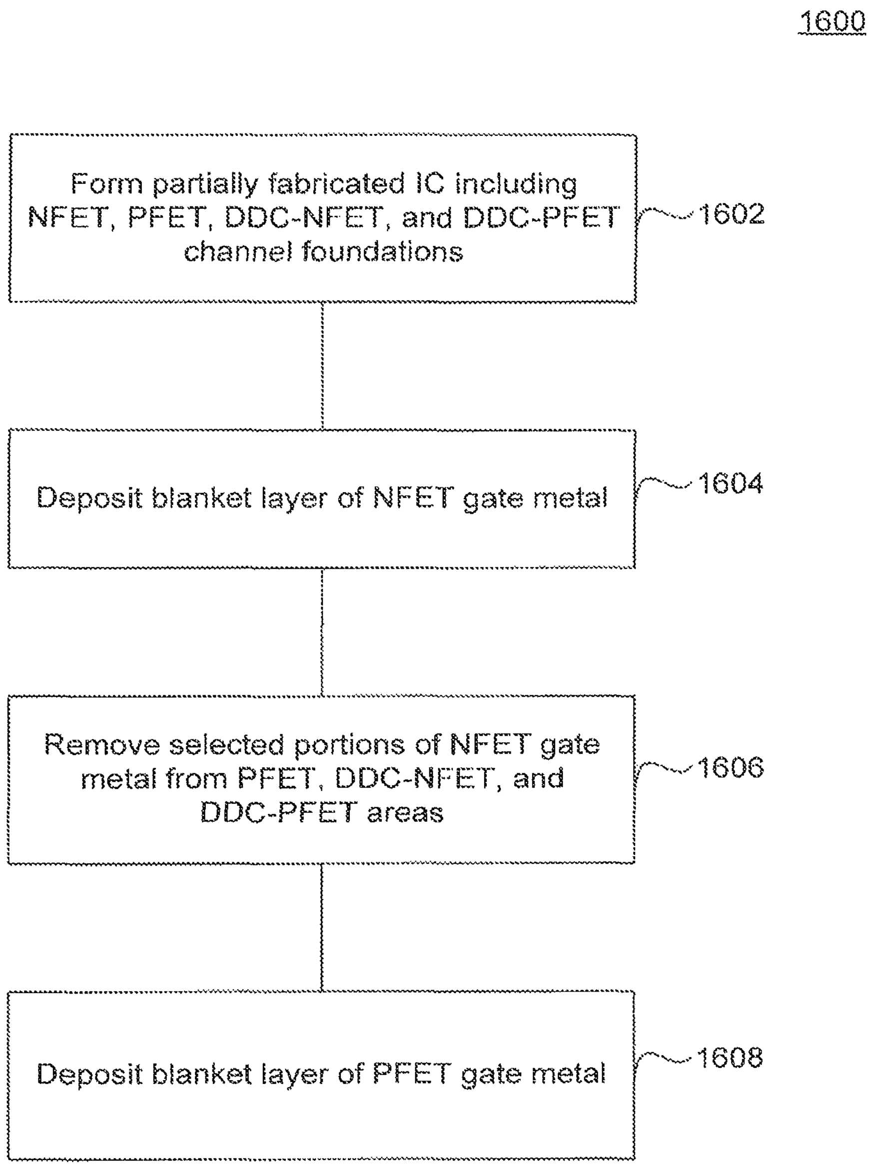

1600
Form partially fabricated IC including NFET, PFET, DDC-NFET, and DDC-PFET channel foundations
1602
Deposit blanket layer of NFET gate metal
1604
Remove selected portions of NFET gate metal from PFET, DDC-NFET, and DDC-PFET areas
1606
Deposit blanket layer of PFET gate metal
1608

FIG. 16

INTEGRATED CIRCUITS HAVING A PLURALITY OF HIGH-K METAL GATE FETS WITH VARIOUS COMBINATIONS OF CHANNEL FOUNDATION STRUCTURE AND GATE STACK STRUCTURE AND METHODS OF MAKING SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. application Ser. No. 13/755,887 filed Jan. 31, 2013 and entitled "Integrated Circuits Having a Plurality of High-K Metal Gate FETs With Various Combinations of Channel Foundation Structure and Gate Stack Structure and Methods of Making Same" which claims the benefit of earlier filed U.S. provisional application No. 61/593,062, entitled "Integrated Circuits Having a Plurality of High-K Metal Gate FETs With Various Combinations of Channel Foundation Structure and Gate Stack Structure and Methods of Making Same" filed 31 Jan. 2012, and incorporated herein by reference in its entirety.

INCORPORATION BY REFERENCE OF ADDITIONAL DOCUMENTS

The following are incorporated herein by reference: U.S. patent application Ser. No. 12/708,497, filed 18 Feb. 2010, titled "Electronic Devices and Systems, and Methods for Making and Using the Same," by Scott E. Thompson et al., now U.S. Pat. No. 8,273,617; U.S. patent application Ser. No. 12/971,884, filed 17 Dec. 2010, titled "Low Power Semiconductor Transistor Structure and Method of Fabrication Thereof;" U.S. patent application Ser. No. 12/971,955, filed 17 Dec. 2010, titled "Transistor with Threshold Voltage Set Notch and Method of Fabrication Thereof;" U.S. patent application Ser. No. 12/895,785, filed 30 Sep. 2010, titled "Advanced Transistors With Threshold Voltage Set Dopant Structures;" U.S. patent application Ser. No. 12/960,266, filed 3 Dec. 2010, titled "Semiconductor Structure and Method of Fabrication Thereof with Mixed Metal Types;" and U.S. patent application Ser. No. 13/459,971, filed 30 Apr. 2012, titled "Multiple Transistor Types Formed in a Common Epitaxial Layer by Differential Out-Diffusion From a Doped Underlayer," the disclosures of which are hereby incorporated by reference in their entirety.

FIELD OF THE INVENTION

The present invention relates generally to integrated circuits and processes for making integrated circuits.

BACKGROUND

Advances in semiconductor manufacturing technologies have resulted in dramatically increased circuit packing densities and higher speeds of operation. In order to achieve such increased densities and circuit speeds, a wide variety of evolutionary changes have taken place with respect to semiconductor processing techniques and semiconductor device structures.

Some of the more recent changes in metal-oxide-semiconductor field effect transistor (MOSFET) semiconductor processing and device structures include gate replacement structures and manufacturing methods for such. In gate replacement, conventional polysilicon-based gate stack structures are removed after source/drain formation, and a gate stack with a high-k gate dielectric layer and a metal gate electrode (HKMG) are provided in their place. Various combinations of metals and metal alloys are selected by manufacturers to set a nominal value for the work function of the gate electrode. Such efforts are commonly referred to as work function engineering. It is well-known that the work function of the gate electrode is one of the factors in establishing the threshold voltage of a MOSFET.

In addition to changes in the gate stack structure, changes in the semiconductor body underlying the gate stack have also been adopted. A partial list of these changes includes the use of complex doping profiles, strained silicon, fully depleted silicon-on-insulator, raised source/drains, epitaxial silicon layers and finFET structures.

Typically, a semiconductor manufacturer develops a process, and then provides electrical modeling data and physical layout rules to chip designers. Chip designers, or more commonly the company by which the chip designers are employed, arrange for production of their circuit designs as integrated circuits fabricated by the semiconductor manufacturer.

As new transistor structures become available, where those new structures have certain desirable electrical properties, chip designers often wish to take advantage of those desirable electrical properties in at least some portion, or subset, of the circuitry in an existing chip design. By way of example, System on a Chip (SoC) devices often include blocks of pre-designed circuitry some of which may be supplied from different vendors. In order to get the desired performance from each of those blocks, different transistor characteristics may be needed in the different blocks. Put differently, it may be desirable to include a plurality of transistor types having various combinations of channel structures and gate stacks.

What is needed are integrated circuits with multiple transistor structures, each with its own unique electrical characteristics, and methods of integrating the manufacture thereof into a single process flow.

BRIEF DESCRIPTION OF THE DRAWINGS

Exemplary embodiments of the invention are described with reference to the accompanying drawings. In the drawings, like reference numbers indicate identical or functionally similar elements.

FIG. **1** is a cross-sectional representation of a portion of a wafer having a partially fabricated integrated circuit thereon in accordance with a baseline process.

FIG. **2** shows the structure of FIG. **1** after a dummy gate stack has been removed and a high-k gate dielectric is formed on the surface exposed by removal of the dummy gate stack.

FIG. **3** shows the structure of FIG. **2** after deposition of a blanket layer of tantalum nitride (TaN).

FIG. **4** shows the structure of FIG. **3** after selected portions of the TaN are removed from PFET areas of the integrated circuit, but remains in NFET gate stacks areas.

FIG. **5** shows the structure of FIG. **4** after deposition of a blanket layer of titanium nitride (TiN).

FIG. **6** shows the structure of FIG. **5** after a chemical mechanical polishing (CMP) operation has removed the excess Al, TiN and TaN from the upper surface of a dielectric layer surrounding the gate stack/spacer structures.

FIG. **7** is similar to the structure of FIG. **3**, except Deeply Depleted Channel (DDC) channel foundations are provided for a portion of the NFETs and PFETs, and after selected portions of the blanket layer of TaN are removed such that TaN is removed from the PFET, DDC-NFET, and DDC-PFET areas of the integrated circuit, but remains in the NFET gate stack; and after the deposition of a blanket layer of TiN.

FIG. **8** shows the structure of FIG. **7** after deposition of an Al fill in the gate stacks and after a chemical mechanical polishing operation has removed the excess TiN and TaN from the upper surface of a dielectric layer surrounding the gate stack/spacer structures.

FIG. **9** is similar to the structure of FIG. **3**, except DDC channel foundations are provided for a portion of the NFETs and PFETs, and after selected portions of the blanket layer of TaN are removed such that TaN is removed from the PFET areas of the integrated circuit, but remains in the NFET, DDC-NFET and DDC-PFET gate stacks.

FIG. **10** shows the structure of FIG. **9** after deposition of an Al fill in the gate stacks and after a chemical mechanical polishing operation has removed the excess TiN and TaN from the upper surface of a dielectric layer surrounding the gate stack/spacer structures.

FIG. **11** is similar to the structure of FIG. **2**, except DDC channel foundations are provided for a portion of the NFETs and PFETs, and after deposition of a blanket layer of TiN_x, removal of selected portions of the TiN_x such that TiN_x is removed from the NFET and PFET areas, but remains in the DDC-NFET and DDC-PFET gate stacks.

FIG. **12** shows the structure of FIG. **11** after deposition of a blanket layer of TaN.

FIG. **13** shows the structure of FIG. **12** after selected portions of the TaN blanket layer have removed such that TaN is removed from the PFET, DDC-NFET and DDC-PFET areas, but remains in the NFET gate stack.

FIG. **14** shows the structure of FIG. **13** after deposition of a blanket layer of TiN.

FIG. **15** shows the structure of FIG. **14** after deposition of an Al fill in the gate stacks and removal of the excess TiNx, TaN and TiN from the upper surface of a dielectric layer surrounding the gate stack/spacer structures.

FIG. **16** is a flow diagram of an exemplary manufacturing process for formation of transistor metal gate stacks in a "gate first" sequence.

DETAILED DESCRIPTION

The following Detailed Description refers to accompanying drawings to illustrate exemplary embodiments consistent with the invention. References in the Detailed Description to "one exemplary embodiment," "an illustrative embodiment," "an exemplary embodiment," and so on, indicate that the exemplary embodiment described may include a particular feature, structure, or characteristic, but every exemplary or illustrative embodiment may not necessarily include that particular feature, structure, or characteristic. Moreover, such phrases are not necessarily referring to the same exemplary embodiment. Further, when a particular feature, structure, or characteristic is described in connection with an embodiment, it is within the knowledge of those skilled in the relevant art(s) to affect such feature, structure, or characteristic in connection with other embodiments whether or not explicitly described.

The exemplary embodiments described herein are provided for illustrative purposes, and are not limiting. Other embodiments are possible, and modifications may be made to the exemplary embodiments within the spirit and scope of the invention. Therefore, the Detailed Description is not meant to limit the invention. Rather, the scope of the invention is defined only in accordance with the subjoined claims and their equivalents.

The following Detailed Description of the exemplary embodiments will so fully reveal the general nature of the invention that others can, by applying knowledge of those skilled in relevant art(s), readily modify and/or adapt for various applications such exemplary embodiments, without undue experimentation, without departing from the spirit and scope of the invention. Therefore, such adaptations and modifications are intended to be within the meaning and plurality of equivalents of the exemplary embodiments based upon the teaching and guidance presented herein. It is to be understood that the phraseology or terminology herein is for the purpose of description and not of limitation, such that the terminology or phraseology of the present specification is to be interpreted by those skilled in relevant art(s) in light of the teachings herein.

TERMINOLOGY

The terms, chip, die, integrated circuit, semiconductor device, and microelectronic device, are often used interchangeably in the field of electronics. The present invention is applicable to all the above as these terms are generally understood in the field.

With respect to chips, it is common that power, ground, and various signals may be coupled between them and other circuit elements via physical, electrically conductive connections. Such a point of connection may be referred to as an input, output, input/output (I/O), terminal, line, pin, pad, port, interface, or similar variants and combinations. Although connections between and amongst chips are commonly made by way of electrical conductors, those skilled in the art will appreciate that chips and other circuit elements may alternatively be coupled by way of optical, mechanical, magnetic, electrostatic, and electromagnetic interfaces.

The terms metal line, trace, wire, conductor, signal path and signaling medium are all related. The related terms listed above, are generally interchangeable, and appear in order from specific to general. In this field, metal lines are sometimes referred to as traces, wires, lines, interconnect or simply metal. Metal lines, such as aluminum (Al), copper (Cu), an alloy of Al and Cu, an alloy of Al, Cu and silicon (Si), tungsten (W), and nickel (Ni) are conductors that provide signal paths for coupling or interconnecting, electrical circuitry. Other conductors, both metal and non-metal are available in microelectronic devices. Materials such as gold (Au), cobalt (Co), doped polysilicon, doped single-crystal silicon (often referred to simply as diffusion, regardless of whether such doping is achieved by thermal diffusion or ion implantation), titanium (Ti), molybdenum (Mo), and refractory metal silicides are examples of other conductors.

Polycrystalline silicon is a nonporous form of silicon made up of randomly oriented crystallites or domains. Polycrystalline silicon is often formed by chemical vapor deposition from a silicon source gas or other methods and has a structure that contains large-angle grain boundaries, twin boundaries, or both. Polycrystalline silicon is often referred to in this field as polysilicon, or sometimes more simply as poly.

Epitaxial layer refers to a layer of single crystal semiconductor material. In this field, the epitaxial layer is commonly referred to "epi."

FET, as used herein, refers to field effect transistor. An n-channel FET is referred to herein as an NFET. A p-channel FET is referred to herein as a PFET. Unless noted otherwise the FETs referred to herein are MOSFETs rather than junction FETs (JFETs).

As used herein, "gate" refers to the insulated gate terminal of a FET. The insulated gate terminal of a FET is also referred to in this field as a "gate electrode." Historically, the gate electrode was a single structure such as a layer of doped polysilicon disposed on the gate dielectric. More recently, semiconductor manufacturing processes have used several layers of various materials to produce the desired electrical characteristics.

Source/drain (S/D) terminals refer to the terminals of a FET, between which conduction occurs under the influence of an electric field, subsequent to the inversion of the semiconductor surface under the influence of an electric field resulting from a voltage applied to the gate terminal of the FET. Generally, the source and drain terminals of a FET are fabricated such that they are geometrically symmetrical. With geometrically symmetrical source and drain terminals it is common to simply refer to these terminals as source/drain terminals, and this nomenclature is used herein. Designers often designate a particular source/drain terminal to be a "source" or a "drain" on the basis of the voltage to be applied to that terminal when the FET is operated in a circuit.

The expression "gate stack" refers to the gate electrode and the gate dielectric that separates the gate electrode from the semiconductor body.

The term "channel" as used herein refers to a three-dimensional region of mobile carriers formed subjacent to the interface between the substrate and the gate stack of a FET responsive to application of an electric field to the gate electrode.

The expression "depletion region" as used herein refers to a three-dimensional region subjacent to the gate stack of a FET where that region has been depleted of mobile charges leaving, in a doped region of the body, ionized dopant sites. The depletion region forms responsive to the application of an electric field. It is noted that the size of the depletion region is a related to the doping profile in the region and the applied voltage. In a conventional NFET with a p-type body, the depletion region is characterized by ionized non-mobile acceptor sites. In a conventional PFET with an n-type body, the depletion region is characterized by ionized non-mobile donor sites.

The expression "channel foundation structure" refers to the crystalline structure and doping profile of the body subjacent to the gate stack, together with the S/D structures.

The expression "DDC channel foundation" refers to a channel foundation structure with an undoped, or substantially undoped, epi layer disposed subjacent the gate dielectric layer, a doped threshold adjustment epi layer disposed subjacent the undoped epi layer, and a highly doped screening region disposed subjacent the threshold adjustment layer. Various DDC channel foundation structures may include one or more dopant layers, including but not limited to carbon (C) especially in the case of DDC-NFETs, for reducing or eliminating migration of other dopant species upward into the undoped epi.

The term "high-k" refers to a dielectric constant greater than that of silicon dioxide.

Together, a gate stack disposed adjacent to a channel foundation structure forms a FET.

Together, a gate stack disposed adjacent to a DDC channel foundation forms a DDC-FET. A p-channel DDC-FET is referred to herein as a DDC-PFET. An n-channel DDC-FET is referred to herein as a DDC-NFET.

The terms contact and via, both refer to structures for electrical connection of conductors from different levels of a chip. By way of example and not limitation, such electrical connections may be made between two metal lines on different interconnect levels of a chip, between a polysilicon line and a metal line, between a S/D junction and a metal line, and so on. These terms are sometimes used in the art to describe both an opening in an insulator in which the structure will be completed, and the completed structure itself. For purposes of this disclosure, contact and via both refer to the completed structure. Further, for purposes of this disclosure, contact refers to the structure used to form a connection between the first layer of metal and electrically conductive structures closer to the substrate; and via refers to the structure used to form a connection between metal layers including the first metal layer and the metal layers above it.

Substrate, as used herein, refers to the physical object that is the basic workpiece that is transformed by various process operations into the desired microelectronic configuration. A substrate may also be referred to as a wafer. Wafers, may be made of semiconducting, non-semiconducting, or combinations of semiconducting and non-semiconducting materials (e.g., a silicon-on-insulator (SOI) wafer).

The term vertical, as used herein, means substantially perpendicular to the surface of a substrate.

Overview

As noted above, chip designers often wish to incorporate the latest advances in electrical performance that are obtainable through the use of newly available transistor structures, without necessarily moving the entire chip design to a smaller technology node. This is often the case where the new transistor structure is available at the same technology node (i.e., manufacturing dimensions) as an existing design. By way of example, the transistors that make up a particular circuit block such as a memory could be replaced with the new transistor structures to achieve the desired electrical result without having to modify other circuits that have already been validated.

One family of newly available transistor structures is referred to herein as DDC-FETs. DDC-FETs have a number of advantages in terms of electrical performance over conventional FETs at the same technology node. These advantages include, but are not in any way limited to, reduced subthreshold conduction (i.e., reduced off-state leakage current). Because modern integrated circuits typically include many millions of transistors, even small amounts of leakage current in these transistors rapidly becomes a drain on the battery of a mobile device, and/or a heat dissipation problem requiring heavy, and space-consuming heat sinks or fans.

DDC-FETs are also advantageous in terms of reduced threshold voltage variation across a given region of an integrated circuit. This type of threshold voltage variation is referred to as sigma V_t (σV_t). Circuit designers recognize the many well-known benefits of reduced variation (or increased uniformity) in the electrical characteristics of the devices that are available for them to incorporate into their designs. By way of example and not limitation, the use of devices with a smaller variation in electrical characteristics can provide circuit designs with improved performance margins.

Since it is desirable to reduce power, and to improve performance margins, as soon as is practical, there is a desire to begin the change-over to DDC-FETs as soon as possible. At the same time, because of the expense involved in validating a new design, generating mask sets, and making or purchasing wafers, some chip designers prefer to make changes in stages. In accordance with such a philosophy, chip designers may decide to replace only portions of a chip design with the newly available DDC-FETs.

Additionally, chip designers producing SoCs (System On a Chip) often license-in various "IP" blocks, i.e., pre-designed circuit blocks having a known function. In some license arrangements it might not be permitted for the chip designers to make changes to such a licensed circuit block. In accordance with such a contractual limitation, chip designers may decide to replace only portions of a chip design with the newly available DDC-FETs.

In order to satisfy the above-described needs and constraints, it is necessary to combine multiple transistor architectures, or structures, within the same integrated circuit.

In order to maintain the economic feasibility of combining multiple transistor architectures within an integrated circuit, new process flows have been developed by the inventors that provide cost-effective integration of multiple transistor structures within an integrated circuit. Various illustrative embodiments of such novel and non-obvious processes are set forth below.

In various embodiments, DDC-FETs are incorporated into an integrated circuit that includes FETs of alternative structures, or architectures. DDC refers to the channel region of a FET that has been physically constructed to provide a desired set of electrical characteristics, including but not limited to higher mobility, higher drive current, lower drain induced barrier lowering ("DIBL") and reduced threshold voltage variations.

In order to facilitate the description of the combinations of different transistor structures, the FETs are often described herein in terms of their channel foundation structure, and their gate stack structure. A plurality of different transistor structures are compatibly integrated by a process flow to produce integrated circuit structures and circuits as illustrated in exemplary embodiments herein. Various embodiments are described herein where HKMG FETs are fabricated in a gate-last style of gate replacement processing, and where the channel foundation and the gate stack structure are mixed and matched on a single integrated circuit. In this way, DDC FETs may be integrated with conventional FETs independent of a particular gate-stack architecture.

Process

FIGS. **1-15** illustrate a process flow including process options for gate stack formation. These process options allow the integration of both NFETs and PFETs where each transistor type may have a different channel foundation structure and/or a different gate stack. In other words, various embodiments provide integrated circuits that combine conventional transistors and DDC transistors, and optional combinations of gate stacks so as to simplify processing while delivering the desired electrical characteristics.

Various embodiments provide for re-use of at least a portion of the available gate stack materials and structures available in semiconductor manufacturing. This simplifies manufacturing. Rather than fabricating a unique gate stack structure for each type of transistor on an integrated circuit, the gate stack materials and structure, together with the transistor's underlying channel foundations, are selected such that at least two different types of transistor can use the same gate stack materials and structure. In this way, the same gate stack structure can be concurrently fabricated for the at least two different types of transistors. As described below, gate stack materials and structure affect the threshold voltage of a transistor. Thus embodiments provide integrated circuits that have more transistor types than gate stack types.

In the process embodiments herein, even though the process steps are described as being performed in a stated order, particular process steps may be performed at different points in the process flow and in a different order with respect to other process steps as desired to achieve a similar resulting structure. In addition, one or more process steps can be substituted with alternative process steps that can also achieve a similar resulting structure. For example, the process steps of depositing a blanket layer of a gate metal and removing portions of the deposited gate metal from selected areas can be substituted with a process of selectively depositing the gate metal layer such that it is not deposited in the selected areas.

FIGS. **1-6** illustrate an exemplary baseline process where: all the FETs are non-DDC FETs; all the NFET gate stacks use a first common structure; all the PFET gate stacks use a second common structure; and the first and second common structures are different from each other. FIGS. **1-3** and **7-8** illustrate an exemplary process in which: DDC and non-DDC FETs are both present in an integrated circuit; and both the DDC-NFET and the DDC-PFET use the same gate stack structure as the non-DDC-PFET. FIGS. **1-3** and **9-10** illustrate another exemplary process in which: DDC and non-DDC FETs are both present in an integrated circuit, and both the DDC-NFET and the DDC-PFET use the same gate stack structure as the non-DDC-NFET. FIGS. **1-2** and **11-15** illustrate a further exemplary process in which: DDC and non-DDC FETs are both present in an integrated circuit; both the DDC-NFET and the DDC-PFET use the same gate stack structure as each other; and the gate stack of the DDC FETs is different from either the NFET gate stack or the PFET gate stack.

It is noted that the structures shown in FIGS. **7-15** include DDC channel foundations for a DDC-NFET and a DDC-PFET. When referred to in combination with FIGS. **7-15**, the illustrative cross-sectional representations of FIGS. **1-3** are understood to include the DDC channel foundations shown in FIGS. **7-15**, since those figures and the process steps involved are the same except for the formation of the DDC channel foundation, which is described and shown in U.S. patent application Ser. No. 13/459,971, filed 30 Apr. 2012, titled "Multiple Transistor Types Formed in a Common Epitaxial Layer by Differential Out-Diffusion From a Doped Underlayer (incorporated by reference above).

Unless otherwise stated, the figures are representative and not drawn to scale. Those skilled in the art of semiconductor manufacturing readily understand the meaning of such cross-sectional representative figures.

Table 1, shown below, illustrates various non-limiting combinations of channel foundation structures and combinations of gate stack materials.

TABLE 1

	NFET (non-DDC) Channel Foundation	PFET (non-DDC) Channel Foundation	NFET (DDC) Channel Foundation	PFET (DDC) Channel Foundation
Gate Stack Combo	Gate Stack 1	Gate Stack 2		
Gate Stack Combo	Gate Stack 1	Gate Stack 2	Gate Stack 2	Gate Stack 2
Gate Stack Combo	Gate Stack 1	Gate Stack 2	Gate Stack 1	Gate Stack 1
Gate Stack Combo	Gate Stack 1	Gate Stack 2	Gate Stack 3	Gate Stack 3

Illustrative Gate Stack 1 includes: a high-k gate dielectric layer, typically hafnium oxide (HfO); a layer of tantalum nitride (TaN) disposed on the inner surfaces of a sidewall spacer structure, and further disposed over the high-k gate dielectric layer; a layer of TiN disposed over the TaN layer; and a layer of aluminum (Al) disposed over the TaN.

Illustrative Gate Stack 2 includes: a high-k gate dielectric layer, typically hafnium oxide (HfO); a layer of TiN disposed on the inner surfaces of a sidewall spacer structure, and further disposed over the high-k gate dielectric layer; and a layer of Al disposed over the TiN_x.

Illustrative Gate Stack 3 includes: a high-k gate dielectric layer, typically hafnium oxide (HfO); a layer of TiN_x disposed on the inner surfaces of a sidewall spacer structure, and further disposed over the high-k gate dielectric layer; a layer of TIN disposed over the TiN_x; and a layer of Al disposed over the TiN.

It is noted that those skilled in the art and having the benefit of this disclosure will be able to select materials and their respective thicknesses to achieve various desired sets of electrical properties. It is further noted that descriptions of particular metals associated with transistor types are provided to facilitate an understanding of similarities and differences in the gate stacks; but generally, it is understood by those skilled in the art that certain metal material combinations are selected to provide work functions desirable for NFET devices and PFET devices, whether such material combinations are achieved by the materials specified in this disclosure or not. The present invention is not limited to the exemplary gate stacks described above.

A baseline process is first described. Referring to FIG. **1**, a cross-sectional representation of a portion of a wafer **102** having a partially fabricated integrated circuit thereon is shown. The partially fabricated integrated circuit of FIG. **1** show two NFETs **750** and two PFETs **752**. More particularly, FIG. **1** shows: shallow trench isolation (STI) structures **104**; PFETs **752** having silicon germanium (SiGe) raised S/Ds **106**, source drain extensions (SDE) **108**, dielectric layer **114**, polysilicon gate **116**, and sidewall spacers **118**; NFETs **750** having S/Ds **110**, SDEs **112**, dielectric layer **114**, polysilicon gate **116**, and sidewall spacers **118**; and a dielectric layer **120** deposited over the surface of wafer **102** and surrounding sidewall spacers **118**. It is noted that sidewall spacers **118** are formed from dielectric material. It is noted that the SiGe raised S/Ds are sometimes referred to as embedded SiGe (e-SiGe) S/Ds. It is further noted that the present invention is not limited to implementation of PFETs using the raised S/D structures, nor limited to the use of SiGe in the PFET S/D structures. Those skilled in the art and having the benefit of the present disclosure will understand that other PFET S/DI) structures (e.g., planar and finFET) have been, and continue to be used in the semiconductor industry.

In some embodiments halo implants are performed to implant dopants into the channel regions of the NFETs and the PFETs. Such implants are typically performed to set the threshold voltage of the various transistors.

FIG. **2** shows the structure of FIG. **1** after the dummy gate stack (i.e., polysilicon **116**, and dielectric layer **114**) has been removed from each transistor, and a high-k gate dielectric **202** is formed on the surface exposed by the removal of the dummy gate stack. Any suitable etch chemistry may be used to remove the dummy gate stack. In typical embodiments, high-k gate dielectric **202** is hafnium oxide, but the present invention is not limited to gate dielectric layers having any particular chemical composition. Further the present invention is not limited to gate dielectric layers having a uniform chemical make-up. Still further, the present invention comprehends the use of gate dielectric structures in the form of laminates, i.e., two or more layers each having a different chemical composition. Additionally, there may be an interfacial silicon oxide layer (not shown) having a thickness on the order of five angstroms disposed between wafer **102** and gate dielectric layer **202**.

FIG. **3** shows the structure of FIG. **2** after deposition of a blanket layer of tantalum nitride (TaN) **302**. An atomic layer deposition (ALD) technique is typically used to deposit TaN **302**, but any suitable equipment and process conditions may be used, and the present invention is not limited to the particulars of the deposition process.

FIG. **4** shows the structure of FIG. **3** after selected portions of TaN layer **302** are removed such that TaN is removed from the PFET **752** areas of the integrated circuit, but remains in the NFET **750** gate stacks.

FIG. **5** shows the structure of FIG. **4** after deposition of a blanket layer of titanium nitride (TiN) **502**. As can be seen in FIG. **5**, TiN layer **502** covers TaN **302**, and the exposed portions of dielectric layer **120**, sidewall spacers **118**, and gate dielectric layer **202**. The thicknesses of TaN **302** and TiN **502** are selected to provide the desired work function. It is noted that the invention is not limited to any particular method of achieving the desired thicknesses of any materials. It is particularly noted that setting the work function of the gate stack by means of thickness (i.e., not just material selection) can be achieved in any suitable manner including but not limited to controlling the deposition process, or by depositing a greater thickness than desired and the etching back the excess amount of material.

FIG. **6** shows the structure of FIG. **5** after a chemical mechanical polishing operation has removed the excess TiN and TaN from the upper surface of dielectric layer **120**, and the gate stacks are completed with an aluminum filling. The baseline process shows two NFETs **750** each having a gate stack comprised of a hafnium oxide gate dielectric **202**, TaN **302**, TiN **502**, and Al **602**; and two PFETs **752** each having a gate stack comprised of a hafnium oxide gate dielectric **202**, TiN **502**, and Al **602**.

FIG. **7** is similar to the structure of FIG. **3**, except modified to show DDC channel foundations provided for a portion of the NFETs and PFETs. FIG. **7** shows modified FIG. **3** after selected portions of TaN layer **302** are removed such that TaN is removed from the PFET **752**, DDC-NFET **754**, and DDC-PFET **756** areas of the integrated circuit, but remains in the NFET **750** gate stack; and after the deposition of a blanket layer of TiN **708**. Referring again to the DDC channel foundations, DDC-NFET **754** includes an undoped region **706*a*** disposed subjacent high-k gate dielectric layer **202**, a threshold adjustment region **704*a*** disposed subjacent region **706*a***, and a screening region **702*a*** disposed subjacent threshold adjustment region **704*a***. DDC-PFET **756** includes an undoped region **706*b*** disposed subjacent high-k gate dielectric layer **202**, a threshold adjustment region **704*b*** disposed subjacent region **706*a***, and a screening region **702*b*** disposed subjacent threshold adjustment region **704*b***.

It is noted that although various materials are referred to as being "deposited," any suitable equipment and process steps may be used to dispose the materials as indicated herein.

FIG. **8** shows the structure of FIG. **7** after deposition of Al **802** to fill in the gate stacks and after a chemical mechanical polishing operation has removed the excess TiN and TaN from the upper surface of dielectric layer **120**. FIG. **8** illustrates a process and structure in which NFETs and PFETs (**750** and **752** respectively), together with DDC-NFETs and DDC-PFETs (**754** and **756** respectively), are integrated within an integrated circuit. It is noted that only two gate stack structures are used amongst the four types of transistor structures (i.e., the NFET, PFET, DDC-NFET, and DDC-PFET each have a different channel foundation). In this illustrative embodiment, a single type of gate stack is used for PFET **752**, DDC-NFET **754**, and DDC-PFET **756**, while a separate type of gate stack is used for NFET **750**.

FIG. **9** is similar to the structure of FIG. **3**, except DDC channel foundations are provided for a portion of the NFETs and PFETs, and after selected portions of TaN layer **302** are removed such that TaN is removed from the PFET **752** areas of the integrated circuit, but remains in the NFET **750**, DDC-NFET **754** and DDC-PFET **756** gate stacks, and a blanket layer of TiN **902** is deposited.

FIG. **10** shows the structure of FIG. **9** after deposition of Al **1002** to fill in the gate stacks and after a chemical mechanical polishing operation has removed the excess TiN and TaN from the upper surface of dielectric layer **120**, which surrounds the gate stack/spacer structures. It is noted that only two gate stack structures are used amongst the four types of transistor structures. In this illustrative embodiment, a single type of gate stack is used for NFET **750**, DDC-NFET **754**, and DDC-PFET **7565**, while a separate type of gate stack is used for PFET **752**.

FIG. **11** is similar to the structure of FIG. **2**, except DDC channel foundations are provided for a portion of the NFETs and PFETs, and after deposition of a blanket layer of TiN_x, a stochiometric variance of TiN which can modulate the transistor work function, removal of selected portions of the TiN_x blanket layer such that TiN_x is removed from the NFET **750** and PFET **752** areas, but remains in the DDC-NFET **754** and DDC-PFET **756** gate stacks, thus forming patterned TiN_x layer **1102**.

FIG. **12** shows the structure of FIG. **11** after deposition of a blanket layer of TaN **1202**.

FIG. **13** shows the structure of FIG. **12** after selected portions of TaN **1202** have removed such that TaN is removed from the PFET **752**, DDC-NFET **754** and DDC-PFET **756** areas, but remains in the NFET **750** gate stack.

FIG. **14** shows the structure of FIG. **13** after deposition of a blanket layer of TiN **1402**.

FIG. **15** shows the structure of FIG. **14** after deposition of Al **1502** to fill in the gate stacks, and removal of the excess TiNx, TaN and TiN from the upper surface of dielectric layer **120**. The resulting structures are discussed below.

It is noted that conventional processing for metallization and via formation may be performed to complete the integrated circuit subsequent to the completion of the gate stacks.

Even though various process and structure embodiments are described above with reference to re-using gate metals in a gate last process, such gate metal re-use is also applicable to a gate first process. For example, FIG. **16** shows a gate first process flow **1600** that re-uses the PFET non-DDC gate metal for the DDC-NFET and DDC-PFET transistors. At step **1602**, the integrated circuit is partially fabricated in that the NFET, PFET, DDC-NFET and DDC-PFET channel foundations are established, including the formation of a blanket epitaxial layer after doping the channel regions. Then, the gate foundation is patterned so that the metal portions can be formed. For the metal portions, first, in the example at **1600**, an NFET gate metal is deposited across the surface of the patterned gate foundation **1604**. Then, selected portions of NFET gate metal are removed from the PFET, DDC-NFET and DDC-PFET areas **1606**. Then, a layer of PFET gate metal is deposited across the surface of the patterned gate foundation **1608**. Note that an alternative gate first process flow can re-use the non-DDC NFET gate metal for both the DDC-NFET and DDC-PFET transistors. Alternative gate first process flows can use either one or two DDC gate metals having work functions selected to meet threshold voltage requirements for the device, wherein the selected metal may be of the same work function as one of the non-DDC transistors or may be of a different work function.

In either a gate-first process or a gate-last process, the selected DDC gate metal can be used for both the DDC-NFET and DDC-PFET transistors, which may be the same metal as used for the NFET or PFET transistor or may be an alternative metal stack from either NFET or PFET transistors, or, a first metal can be selected for the DDC-NFET transistor and a second metal can be selected for the DDC-PFET transistor, which metal selections may match those used for the NFET and PFET. To achieve different work functions, different metal materials or composites may be used, or the work functions of one or more of the already deposited gate metals (e.g., the non-DDC NFET and/or PFET gate metals, or the one or more DDC gate metals) can be adjusted using techniques such as alloying, ion implantation, post-deposition treatment, thickness adjustment, etc. Techniques for adjusting the metal gate work function using thickness adjustment can also include adjusting the gate metal thickness using selective etch-back, such as performing selective etch-back to adjust the thickness of a first type of gate metal before depositing a second type of gate metal over the first type gate metal.

Structure

FIG. **8**, discussed above in connection with an illustrative process flow, shows the structure of a partially fabricated integrated circuit in which an NFET **750** and a PFET **752**, each having a conventional channel foundation, are formed on the same die as a DDC-NFET **754** and a DDC-PFET **756**, each having the DDC channel foundation. In this embodiment there are four distinct types of transistor, yet only two different gate stacks are needed. NFET **750** has a gate stack including successive layers of hafnium oxide **202**, tantalum nitride **302**, titanium nitride **708** and aluminum **802**, whereas the PFET **752**, DDC-NFET **754**, and DDC-PFET **756** each have the same gate stack, i.e., hafnium oxide **202**, titanium nitride **708** and aluminum **802**. It will be appreciated that the embodiment of FIG. **8** is illustrative and not meant to specifically limit the invention.

FIG. **10**, discussed above in connection with an illustrative process flow, shows the structure of a partially fabricated integrated circuit in which an NFET **750** and a PFET **752**, each having a conventional channel foundation, are formed on the same die as a DDC-NFET **754** and a DDC-PFET **756**, each having the DDC channel foundation. In this embodiment there are four distinct types of transistor, yet only two different gate stacks are needed. PFET **752** has a gate stack having successive layers of hafnium oxide **202**, titanium nitride **902** and aluminum **1002**, whereas NFET **750**, DDC-NFET **754**, and DDC-PFET **756** each have the same gate stack, i.e., successive layers hafnium oxide **202**, tantalum nitride **302**, titanium nitride **902** and aluminum **1002**. It will be appreciated that the embodiment of FIG. **10** is illustrative and not meant to specifically limit the invention.

FIG. **15**, discussed above in connection with an illustrative process flow, shows the structure of a partially fabricated integrated circuit in which an NFET **750** and a PFET **752**, each having a conventional channel foundation, are formed on the same die as a DDC-NFET **754** and a DDC-PFET **756**, each having the DDC channel foundation. In this embodiment there are four distinct types of transistor, yet only three different gate stacks are used. NFET **750** has a gate stack having successive layers of hafnium oxide **202**, tantalum nitride **1202**, titanium nitride **1402** and aluminum **1502**; PFET **752** has a gate stack having successive layers of hafnium oxide **202**, titanium nitride **1402** and aluminum **1502**, and DDC-NFET **754** and DDC-PFET **756** each have the same gate stack, i.e., hafnium oxide **202**, TiN_x layer **1102**, titanium nitride **1402** and aluminum **1502**. It will be appreciated that alternative gate stacks having different materials may also provide the desired electrical characteristics.

In typical embodiments, the gate stack of at least one NFET is electrically connected to the gate stack of at least one PFET; and the gate stack of at least one DDC-NFET is electrically connected to the gate stack of at least one DDC-PFET. In this way, CMOS circuits are formed of DDC-FETs and other circuits are formed of non-DDC-FETs.

In one illustrative embodiment, a method includes, forming, in a substrate, an NFET channel foundation, a PFET channel foundation, a DDC-NFET channel foundation, and a DIC-PFET channel foundation; and disposing an NFET gate stack over the NFET channel foundation, disposing a PFET gate stack over the PFET channel foundation, disposing a DDC-NFET gate stack over the DDC-NFET channel foundation, and disposing a DDC-PFET gate stack over the DDC-PFET channel foundation; wherein the DDC-NFET gate stack and the DDC-PFET gate stack are the same, or use similar materials; and wherein the NFET gate stack and the PFET gate stack structures, or materials, are different from each other.

In another illustrative embodiment, a method of manufacturing integrated circuits, includes forming a first type of NFET channel region in a substrate; forming a first type of PFET channel region in the substrate; forming a second type of NFET channel region in the substrate; forming a second type of PFET channel region in the substrate; forming a first type of NFET gate stack over at least a portion of the channel region of the first NFET type; forming a first type of PFET gate stack over at least a portion of the channel region of the first PFET type; forming a second type of NFET gate stack over at least a portion of the channel region of the second NFET type; forming a second type of PFET gate stack over at least a portion of the channel region of the second PFET type; wherein each gate stack is spaced apart from the corresponding underlying channel region by a gate dielectric layer. In some embodiments, the first type of NFET gate stack and the first type of PFET gate stack are different from each other, and the second type of NFET gate stack and the second type of PFET gate stack are the same as each other. These gate stacks may be fabricated concurrently to make them the same. It will be appreciated that any manufacturing process has variations or non-uniformities. Thus references to a material or a structure being the same, means that the nominal value, or manufacturing targets, are the same. Alternatively, the NFET gate stack and the second type of PFET gate stack are fabricated with similar materials.

In one embodiment, the second NFET gate stack and the second PFET gate stack are each the same as the first PFET gate stack. In a further embodiment, the second NFET gate stack and the second PFET gate stack are each the same as the first NFET gate stack. In a still further embodiment, the second NFET gate stack is different from both the first NFET gate stack and the first PFET gate stack; and the second PFET gate stack is different from both the first NFET gate stack and the first PFET gate stack.

Various embodiments advantageously provide methods of modifying an existing chip design to replace a portion of the transistors in the existing chip design with DDC transistors.

Various embodiments advantageously provide methods of adding one or more transistor types to an existing chip design without modifying the dimensions, physical construction, or electrical characteristics of the other transistors.

Various embodiments advantageously provide methods of incorporating a plurality FET types in an integrated circuit where FET type is determined by the combination of channel foundation and gate stack, and where at least a portion of the FETs are DDC transistors.

Various embodiments provide NFETs and DDC-NFETs with the same nominal threshold voltage; and PFETs and DDC-PFETs with the same nominal threshold voltage.

CONCLUSION

It is to be appreciated that the Detailed Description section, and not the Abstract of the Disclosure, is intended to be used to interpret the claims. The Abstract of the Disclosure may set forth one or more, but not all, exemplary embodiments, and thus, is not intended to limit the invention and the subjoined Claims in any way.

It will be apparent to those skilled in the relevant art(s) that various changes in form and detail can be made therein without departing from the spirit and scope of the invention. Thus the invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the subjoined Claims and their equivalents.

What is claimed is:

1. A method of producing an integrated circuit, comprising:
- forming an epitaxial layer on a wafer;
- forming, on an unsingulated die of the wafer, a plurality of first NFETs, each having a first gate stack, and a first nominal threshold voltage;
- forming, on the unsingulated die, a plurality of first PFETs, each having a second gate stack and a second nominal threshold voltage;
- forming, on the unsingulated die, a plurality of second NFETs, each having a third gate stack, and a third nominal threshold voltage;
- forming, on the unsingulated die, a plurality of second PFETs, each having the third gate stack and a fourth nominal threshold voltage;
- wherein the plurality of second NFETs has a channel foundation layer that includes a first heavily doped screening layer below the epitaxial layer, and the plurality of second PFETs has a channel foundation layer that includes a second heavily doped screening layer below the epitaxial layer.

2. The method of claim **1**, further comprising forming a Vt set layer superjacent the screening layer in at least a portion of the second NFETs or second PFETs and prior to forming the epitaxial layer.

3. The method of claim **1**, wherein at least some of the plurality of second NFETs and plurality of PFETs include dopants in the epitaxial layer sufficient to set Vt.

4. A method of forming an integrated circuit, comprising:
- forming, in substrate, a plurality of NFET channel foundations, a plurality of PFET channel foundations, a plurality of DDC-NFET channel foundations, and a plurality DDC-PFET channel foundations;
- forming on the channel foundations, a blanket substantially undoped epitaxial layer; and
- disposing a first NFET gate stack over a first one of the plurality of NFET channel foundations, disposing a first PFET gate stack over a first one of the PFET channel foundations, disposing a first DDC-NFET gate stack over a first one of the DDC-NFET channel foundations, disposing a first DDC-PFET gate stack over a first one of the DDC-PFET channel foundations;
- wherein the first NFET gate stack and the first PFET gate stack are different from each other; and
- wherein each of the NFET, PFET, DDC-NFET and DDC-PFETs are isolated from one another using an isolation structure that is formed after the formation of the blanket substantially undoped epitaxial layer.

5. The method of claim **4**, wherein, the isolation structure is a shallow trench isolation.

6. The method of claim **4**, wherein the first NFET gate stack has a first work function, the first PFET gate stack has a second work function, the first DDC-NFET gate stack has a third work function, the first DDC-PFET gate stack has a fourth work function.

7. The method of claim 6, wherein the first DDC-NFET gate stack and the first NFET gate stack are the same.

8. The method of claim 6, wherein the first DDC-PFET gate stack and the first PFET gate stack are the same.

9. The method of claim 6, wherein the first DDC-NFET gate stack and the first DDC-PFET gate stack are the same.

10. The method of claim 6, wherein the first DDC-NFET gate stack and the first PFET gate stack are the same.

11. The method of claim 6, wherein the first DDC-PFET gate stack and the first NFET gate stack are the same.

12. The method of claim 5, wherein the first DDC-NFET gate stack, and the first DDC-PFET gate stack are not the same.

13. The method of claim 4, wherein the NFET and PFET devices include halo implanted dopants.

14. The method of claim 4, wherein for substantially the same gate length, the channel mobility of the first DDC-NFET is greater than that of the first NFET, and the channel mobility of the first DDC-PFET is greater than that of the first PFET.

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